thereof. The presently disclosed embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims, rather than the foregoing description, and all changes which come within 5 the meaning and range of equivalence of the claims are, therefore, to be embraced therein.

What I claim is as follows:

- 1. A method of producing an isolation groove in a semiconductor device having active regions and the 10 isolation groove being formed between two of the active regions, wherein silicon oxide is formed inside the isolation groove, a dielectric material is formed on said silicon oxide, filling up said isolation groove and the isolation groove is leveled with an outer surface of a 15 silicon substrate, said method comprising the steps of:
 - (a) forming a silicon oxide layer on said substrate;
 - (b) selectively removing a specified region of said silicon oxide layer so as to expose a part of said substrate, said specified region surrounding a sub- 20 sequent groove forming area and having a width of a distance preventing a spread of silicon oxidation in a subsequent process;

(c) forming a silicon nitride layer on said silicon oxide layer and the substrate exposed in step (b);

- (d) etching selectively both said silicon nitride layer and silicon oxide layer exposing the substrate surface corresponding to said groove forming area, leaving said silicon nitride layer on said specified region and above the active region and forming 30 overhanging eaves above said groove forming
- (e) subjecting said exposed substrate to a first anisotropic wet etching so as to form a V-groove, and tropic ion etching so as to form a trench in said

V-groove resulting in formation of said isolation groove using said silicon nitride layer as a mask;

- (f) forming a silicon oxide layer inside said groove;
- (g) filling said isolation groove with dielectric material; and
- (h) removing said dielectric material until said dielectric material is level with said substrate surface, and oxidizing an exposed surface of said dielectric material using said silicon nitride layer as a mask, forming a silicon oxide layer on said dielectric material;
- (i) removing said first and second silicon nitride layers and said silicon oxide layer until the substrate surface in said active region is exposed; and
- (i) forming an additional silicon oxide layer on said exposed substrate surface.
- 2. A method according to claim 1, wherein said substrate having surface crystal orientation (100) is utilized, and said step (e) is carried out by wet etching in alkali solution, whereby a V-shaped groove is formed anisotropically.
- 3. A method according to claim 1, wherein said substrate having surface crystal orientation (100) is utilized, and said step (e) comprises forming said groove by first wet etching in alkali solution, and second anisotropic etching of reactive sputter etching, whereby Y-shaped isolation groove is formed.
- 4. A method according to claim 3, wherein said Yshaped groove penetrates through a silicon epitaxial layer and reaching a silicon base layer therebeneath, both being constituents of said substrate.
- 5. A method according to claim 1, wherein said specified region has a width of greater than 3,000 Angstroms.
- 6. A method according to claim 1, wherein said specifurther subjecting said V-groove to a second aniso- 35 fied region has a width of greater than 3,000 Angstroms.

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